International Journal of Recent Advances in Multidisciplinary Topics
Volume 3, Issue 2, February 2022
https://www.ijramt.com | ISSN (Online): 2582-7839

Review on Design and Analysis of ALU Using Reversible Logic Gates

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***Abstract*: [1] Reversible logic has been of great scientific interest in recent years because of its ability to reduce power dissipation which is the main requirement in low power design. Optimization of power is the primary necessity in portable devices like battery operated devices. It finds its wide range of applications in the fields of Optical computing, Quantum computing, Complementary Metal oxide semiconductor and Nanotechnology. The reversible computing can be performed by using reversible logic gates which perform arithmetic and logical operations. The ALU (Arithmetic Logic Unit) is a digital electronic circuit that conducts operations on binary numbers in arithmetic and bitwise logical ways. It is used to perform all logical and arithmetic function in processors. It is also an important subsystem in digital system design. An ALU has a variety of input and output nets which are used to convey digital signals between the ALU and external circuitry. [4] ALUs which are designed using non reversible logic gates consume more power. So, there is a need for low power consuming ALU designs. This paper is a review of previous works on the design and implementation of ALU using reversible logic gates. The key objective of this work is to analyze the design of the function blocks individually, in order to attain better understanding about reversible computing.**

***Keywords*: Reversible gate, Power optimization, Arithmetic Logic Unit, Feynman gate, Peres gate, Toffoli gate, Fredkin gate, Digital circuits.**

1. Introduction

The Arithmetic Logic Unit is a very important subsystem in the digital system design. It constitutes an integral part of a computer processor that performs arithmetic and logic operations in the computer. An ALU is a combinational logic circuit that can have more inputs and only one output. Nowadays ALU is getting smaller and more complex to enable the development of a smaller but more powerful processors. The need for high speed, less power consumption and compatible processors has been increasing as a result of computer, digital signal processing and networking applications. [3] Reversible logic has received great attention in the recent years due to its ability to reduce the power dissipation which is the main requirement in low power VLSI design. [1] It has wide applications in low power CMOS and Optical information processing, DNA computing, quantum computation and nanotechnology. The important reversible gates used for reversible logic synthesis are Feynman Gate, Fredkin gate, Toffoli gate, and Peres gate.

2. Theory

'Reversibility' in computing implies that no information about the computational states can be lost, so any earlier stage can recovered by computing backwards or un-computing the results. Reversible circuits conserve information by uncomputing bits instead of throwing them away. This is termed as logical reversibility. Logical reversibility and its benefits can only be obtained by employing physical reversibility. Reversible computing offers the only possible physical way to improve performance. It also leads to improvement in energy efficiency. Reversible computing is strongly affected by digital logic designs. Reversible logic elements are needed to recover the state of inputs from the outputs. Reversible logic supports the process of running the system both forward and backward. This means that reversible computations can generate inputs from outputs and can stop and go back to any point in the computation history.

Computing systems give off heat when voltage levels change from positive to negative: bits from zero to one. Most of the energy needed to make that change is given off in the form of heat. Rather than changing voltages to new levels, reversible circuit elements will gradually move charge from one node to the next. This way, one can only expect to lose a minimal amount of energy on each transition. Theoretically physical reversibility is a process that dissipates no energy or heat. *Definition 1*: A reversible gate is a n x n circuit (n inputs and n outputs) which uniquely maps each of its input to its corresponding output. Reversible gates must satisfy the following conditions:

1. It should have equal number of inputs and outputs
2. It should have one to one mapping between the inputs and outputs.
3. There should be neither feedback nor fanout in case of

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a reversible gate.

Definition 2: Ancilla inputs of a reversible gate are the inputs which should be maintained constant at either '0' or '1' so that the gate realizes the required Boolean function.

Definition 3: Garbage outputs of a reversible gate are the extra outputs which are of no logical use and are present only to maintain reversibility.

Definition 4: Quantum cost refers to the cost of the circuit (or gate) in terms of number of 1x1 and 2x2 primitive gates used to design that circuit (or gate).

3. Applications

Reversible computing has applications in transaction processing and computer security, but the main long-term benefit is felt very well in those areas which require high energy efficiency, speed and performance. It finds applications in areas like

1. Low power CMOS.
2. Quantum computer.
3. Nanotechnology
4. Optical computing
5. Design of low power arithmetic and data path for digital signal processing (DSP).
6. Field Programmable Gate Arrays (FPGAs) in CMOS technology for extremely low power, high testability and self-repair.

4. Reversible gates

1) Feynman Gate

Feynman gate is also known as 2X2 reversible gate. The input and output vectors for Feynman gate is in (A, B) and Out (P, Q) respectively. The outputs of FEYMAN gate are denoted as P=A, Q=A XOR B. The application of this gate is used in many circuits because of low cost of the FEYMAN gates. Feynman Gate (FG) can be used as a copying gate. Since a fan-out is not allowed in reversible logic, this gate is useful for duplication of required output.

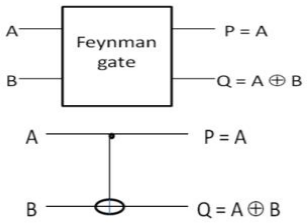
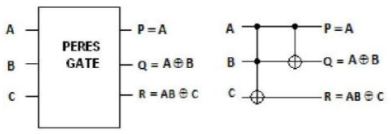


Figure 1: Feynman Gate

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

2) Peres Gate

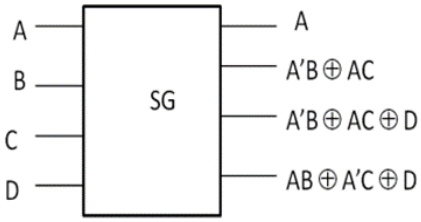
It is a 3X3 reversible gate. Let the input and output for PERES gate be In (A, B, C) and Out(P, Q, R) respectively. The output is defined as P = A, Q = A XOR B and R=AB XOR C. Peres gate is used in many designs because of its lowest quantum cost. Half adder can be designed by using Single Peres gate.

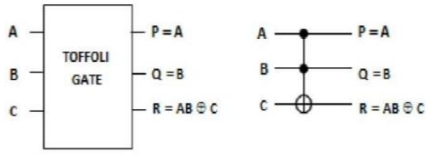


A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

3) Toffoli gate

The following figure shows a 3*3 Toffoli gate. If the input vector is I (A, B, C) and the output vector is O (P, Q, R), then outputs are defined by P=A, Q=B, R=AB ⊕ C



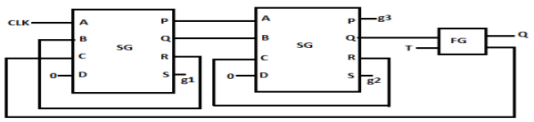


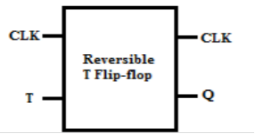
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

4) Sayem Gate

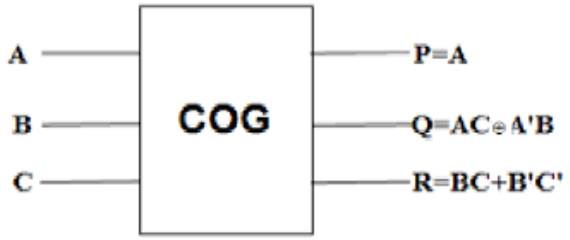
It is a 4x4 reversible gate. The input and output vector of this gate are, Iv = (A, B, C, D) and Ov = (A, A'B ⊕ AC, A'B ⊕ AC⊕ D, AB ⊕ A'C ⊕ D).

5) Reversible Positive Edge Triggered T-Flip Flop





A Master-Slave T Flip-Flop has been designed using reversible gates. The truth table and design are shown below. The added Feynman gate as shown in figure is to get the desired functionality of Q-1.



6) COG Gate

A COG gate is a 3x3 gate with inputs A, B and C and outputs P, Q and R such that P=A, Q=AC XOR A'B and R=BC XOR B'C'. It has a quantum cost of four

7) CNOT Gate

A CNOT (Controlled NOT) is a 2x2 gate which maps its two inputs I1 and I2 to its two outputs Y1 and Y2 such that Y1=I1, Y2=I1 ˙I2. CNOT gate representation is as shown.

5. ALU with irreversible logic gates

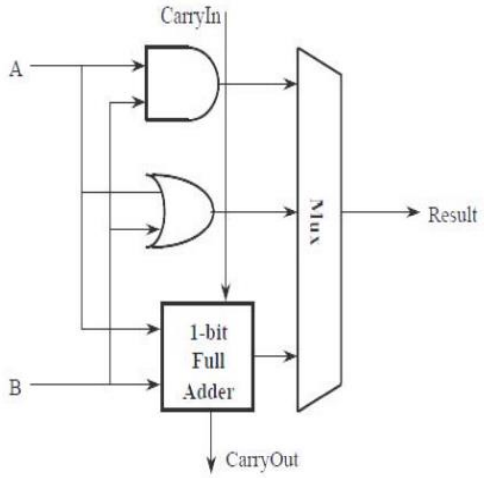
The 16-bit ALU is designed which allows the computer to add, subtract, multiplication and division and to perform basic logical operations such as AND, OR, XOR, XNOR, NAND and inverter etc. A low power 16-bit ALU is designed using Verilog HDL. Verilog HDL is an industry standard language for the description, modelling and synthesis or simulate of digital circuits and systems. In ALU architecture, a high-performance arithmetic hardware with minimum possible clock cycles capable of computing square, square root and inverse in addition to basic arithmetic operations. [2]

The ALU comprises of three units namely arithmetic, logical and control unit. The following subsections focus on the designing of these three units and in the end, all of them are integrated together to form the complete ALU.

1) Arithmetic Unit

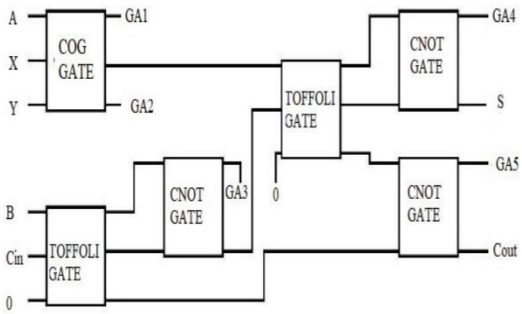
X	Y	Cin	OUTPUT	FUNCTION
0	0	0	B	Transfer B
0	0	1	B plus 1	Increment B
0	1	0	A plus B	Addition
0	1	1	A plus B plus 1	Add with carry
1	0	0	B plus A'	1's Complement subtraction (B-A)
1	0	1	B plus A' plus 1	2's Complement subtraction (B-A)
1	1	0	B minus 1	Decrement B (2's complement decrement)
1	1	1	B	Transfer B

The proposed arithmetic unit has five inputs A, B, Cin, X and Y and two outputs S and Cout. Depending upon the selection bits X and Y and the value of Cin (input carry from previous stage), an operation is being carried out on the inputs A and B. S is the final sum/difference bit produced and Cout is the final carry/borrow bit produced. The functions performed by the arithmetic unit are summarized in Table and the design is depicted:



Functional block diagram of one bit ALU

For a n-bit ALU 'n' of such units are combined to derive one output. Ex: for a 32-bit ALU, A0 to A31 can be the individual 1-bit ALUs. A low power 16-bit ALU is designed using Verilog HDL. Verilog HDL is an industry standard language for the description, modelling and synthesis or simulate of digital circuits and systems. The proposed design 1 has a quantum cost of 17. It has 5 garbage outputs and 2 ancilla inputs.



Design 1 of arithmetic unit

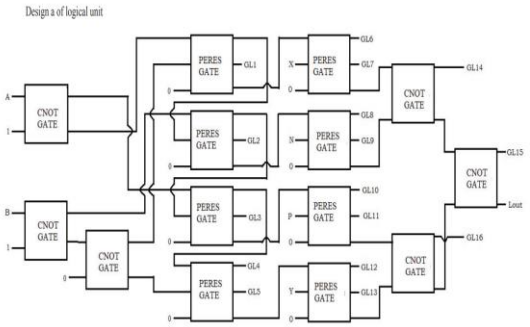
The proposed design 2 has a quantum cost of 13. The number of garbage outputs and ancilla inputs are same as those of Design 1.

2) Logical Unit

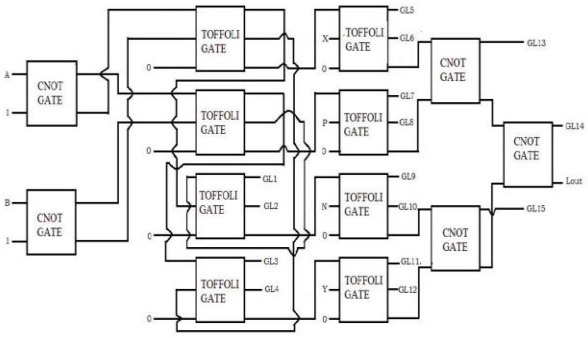
The logical unit has six inputs- A, B, X, Y, N and P. The result of the logical operation performed on the input A and B is reflected on the output bit Lout. The logical operation to be performed is selected by the selection bits X, Y, N and P. The logical unit will have two realizations. The first design (Design a) uses Toffoli and CNOT gates while the second design (Design b) uses Peres and CNOT gates. In each design, GLi represents ith garbage output of the proposed logical unit. 'Design a' has a quantum cost of 45 while it has 15 garbage outputs and 10 ancilla inputs. Design b has a quantum cost of 38. Besides, it has 16 garbage outputs and 11 ancilla inputs.

TABLE II. FUNCTION TABLE OF PROPOSED LOGICAL UNIT

X	Y	N	P	Output
0	0	0	0	0
0	0	0	1	A.B
0	0	1	0	A'.B
0	0	1	1	B
0	1	0	0	A.B'
0	1	0	1	A
0	1	1	0	$A \oplus B$
0	1	1	1	A + B
1	0	0	0	(A + B)'
1	0	0	1	$(A \oplus B)'$
1	0	1	0	A'
1	0	1	1	A' + B
1	1	0	0	B'



3) Design b of logical unit



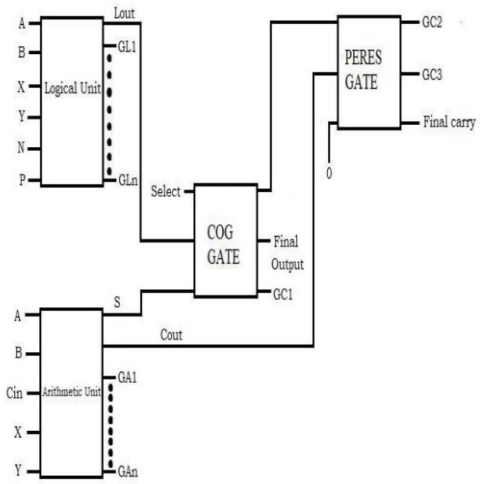
4) Control unit

The final component of the ALU to be designed is the control unit. Control unit decides whether an arithmetic or logical operation has to be performed depending upon the input bit 'Select'. The COG gate will pass the arithmetic unit's result 'S' or the logical unit's result 'Lout' depending upon the Select bit being '1' or '0' respectively. The Cout bit of the arithmetic unit is 'ANDed' with the 'Select' bit so that it is only active when an arithmetic operation is being performed, otherwise, it will remain constant at logic 0 for a logical operation. This 'AND' operation requires a Peres gate. GCi represents ith garbage output of control unit.

5) Final ALU design

The ALU designs are obtained by combining the proposed arithmetic, logical and control units.

The three units of ALU are combines using the connections shown below:



. General structure of proposed ALUs

6. Conclusion

The above-mentioned conclusions are made by extensive literature research and review and it can be concluded that one of the low power technique, Reversible logic gates can be used to reduce the power dissipation as compared to irreversible logic gates. When an ALU is designed using non reversible logic gates, it is said to consume more power of about 0.312 mw and the implementation of ALU based on reversible logic can reduce the power consumption during operations to about 5.1%. The scope for application of this technology is vast and yet to be explored. This paper has drawn these conclusions through thorough case studies and if implemented, the scope for reversible computing is vast.

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