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ULSI Interconnect Scaling: Trends, Challenges and their Solutions

Shefali Madikanti[1*], Kaleem Fatima[2]
[1]Research Scholar, Department of Electronics and Communication Engineering, Osmania University, Hyderabad, India
[2]Professor, Department of Electronics and Communication Engineering, Muffakham Jah College of Engineering and Technology, Hyderabad, India

***Abstract*: Interconnects are the performance limiters in ULSI circuits connecting number of transistors as per Moore's law. Performance of an Integrated Circuits is largely depending on these interconnect's structure where wires are placed closer to each other with high aspect ratios. Today, interconnects account for a substantially bigger proportion of overall latency and expense in integrated circuits than in the past. Interconnect pitch reduction increases layout density but decreases interconnect RC delay. Increasing the metal aspect ratio (thickness/width) improves RC delay, although the best results are obtained when the aspect ratio is around 2. Adding more interconnect layers enhances density and performance, but within a few generations, practical limits are reached. To meet future ULSI connectivity standards, new conductor and dielectric materials, as well as enhanced circuit design methodologies, will be required. In this paper, the trends, challenges and solutions for scaling of interconnects are discussed for achieving high performance in ultra-deep submicron USLI circuits.**

***Keywords*: Interconnect pitch, aspect ratio, RC delay, ULSI, dielectric materials.**

1. Introduction

Over the last decade, there has been considerable improvements in scaling of interconnects in integrated circuits. As expected by Dennard scaling, the delay, power dissipation introduced due to densely packed interconnects and power-delay product which is the overall performance indicator of ULSI circuits shall improve by introducing novel methods of achieving high performance of these scaled interconnects in high-speed ULSI circuits. Using transistor scaling, a concept for simultaneously enhancing transistor density and performance [2], steady advances in integrated circuit density and performance have been proven over the past 20 years. Performance will improve proportionally to feature size until at least the 0.1 µm generation [1]. While transistor scaling is still required, metal interconnects have become a significant limiting factor in ULSI density and performance, and are now as critical as transistors. Assuming a stable metal aspect ratio and no change in conductor or dielectric materials, each technology generation represents a 0.7x reduction in feature size and a 2x increase in connection delay. If typical interconnect scaling is continued, interconnect delay for high frequency devices is already a major fraction of the clock cycle time and will soon exceed the cycle time requirements.

2. Performance of Interconnect Scaling

Interconnect scaling is required for densely packed ULSI circuits. Despite the line length scaling, scaling improves layout density but introduces propagation delay which in otherwise is the signal transmission delay. The resistance and capacitance of a circuit per unit length is expressed as in (1) and (2).

$$\frac{R}{L} = \frac{\rho}{wh} = \frac{4\rho}{aP^2} \tag{1}$$

$$\frac{C_{total}}{L} = 2\frac{(C_L + C_V)}{L} = 2\varepsilon\left(\frac{h}{s} + \frac{w}{t}\right) = 2\varepsilon(a+1) \tag{2}$$

ε is the dielectric constant of the Dielectric material introduced in the metal layer. Considering the metal aspect ratio at fixed constant value, the resistance of an interconnect will increase linearly with the increase in length of the interconnect while the capacitance of the interconnect remains constant. RC delay or in other words propagation delay of signal transmission improves with the increase in metal aspect ratio of wire but this improvement in decrease of RC delay gradually diminishes with the increase in resistance and capacitance of an interconnect for scaled technology nodes.

To achieve better performance of an interconnect at lower cost, connection pitches must be honed. The diminishing of RC delay can be reduced by honing of local interconnect length for density and by honing of global interconnect length for better performance in the interconnect stack. For achieving large density and better performance in ultra-deep submicron ULSI circuits, this combination is essential. For many years, this approach has been employed to reduce the effect of line resistance on circuit delay. The average interconnect stack pitch, omitting the top pitch layer, is shown in Fig. 6 from 65nm to 14nm nodes. At the 45nm process, a thick metal layer is added to the top of the interconnect stack, resulting in increase in connection pitch. As previously proved by an examination of Intel's 1.5m to 0.35m technology [3], this tendency has not changed in more than 20 years.

$$RC = 2\rho\varepsilon\varepsilon_o\left(\frac{4L^2}{P^2} + \frac{L^2}{T^2}\right) \tag{3}$$

*Corresponding author: kaleemfatima@gmail.com

Future technology generations will not benefit from increasing aspect ratio since the reduction in metal resistance will be countered by an increase in lateral capacitance (CL). Interconnect RC delay can be computed as a function of metal thickness and aspect ratio using equation (3). Benefits of increasing aspect ratio for RC delay reduce above aspect ratios of ~ 2.

Interconnect delay will be improved and AC power consumption will be reduced by lowering the dielectric constant of the inter-level dielectric. Many low ε dielectrics, including fluorine doped SiO_2, polymers, and aerogels, are being studied, with the best giving a nearly two-fold drop in [13], [14]. However, finding a low-ε material with the mechanical and reliability features necessary in integrated circuits remains a difficult task. Good adhesion between metal and dielectric layers, resilience during high temperature processing, and the ability to fill tiny spaces between metal lines are examples of such features.

To prevent copper from drifting into the dielectric, copper interconnects require a diffusion barrier. The scaling of resistance as estimated in (1) assumes that the barrier thickness scales as well, and the cross-section of the wire does not consume any additional area. Using of thin barriers of 2nm thickness is one of the approaches for reducing the resistance of the interconnect. Apart from signal transmission delay, the metal film must resist the higher current densities at scaled technology node without electromigration (EM). Low-level metal doping of the Cu connection can boost EM lifespan considerably. For future nodes, new Cu capping techniques that support enhanced EM are also being developed. Because the ideal connector pitch and layer count are highly circuit dependent, multiple connectivity options at scaled technology nodes are being developed to address a wide range of circuit design needs.

To increase the performance of scaled interconnects, new dielectric materials are introduced. Fluorine-doped SiO_2 was first implemented as dielectric material in interconnects [4]. Air-gap technique was added at the 14nm node to considerably improve line-to-line capacitance. SiN was first utilised as the Cu dual-damascene etch-stop layer. Multiple via sizes were implemented at the 65nm process to support decreased via resistance. At the 45nm process, a thick top metal layer was introduced to support global routes and power distribution [9]. At 32nm, planar high-density metal-insulator-metal capacitors were added for improved power droop [10]. Interconnect delay can be reduced by improving process features and materials.

3. Patterning of Interconnects

To achieve high performance of interconnect with improved RC delay in densely packed ULSI circuits, several patterning integration approaches are required. Intel was the first to create a Self-Aligned Via (SAV) technology. The SAV process flow includes a hard mask layer, trench patterning, and finally vias patterning to match the trench width. Because of its ability to work with tight margin, this method has been extended to future technology nodes. For maximizing the contact area and minimizing the wire resistance, SAV approach is the best for densely packed interconnects Intel implemented Self-Aligned Double Patterning (SADP) at the 14nm node to enable a 52nm pitch process. In this method, half of the metal lines are generated where the photoresist is deposited, and the other half are created between the photoresist. To reap the full benefits of density, co-optimization between process and circuit design is required, but the performance benefits of capacitance are obvious.

4. Future Trends

Equation (3) provides performance measurements for interconnects, but to fully address future interconnect scaling requirements, a density metric that includes both connection pitch and layer count is required. Effective metal pitch (P_{eff}), which is defined as, is a proposed density metric.

$$P_{eff} = \frac{P_{avg}}{N} \tag{4}$$

P_{avg} and N for future technology generations can be computed using equations (3) and (4), given particular density (P_{eff}) and performance (RC) targets. P_{eff} should scale at the same rate as the other minimum dimensions, which is typically 0.7 times every generation. Assuming that a metal aspect ratio of 2 is a reasonable upper limit, T=P in equation (3). The length of each line will be assumed to be fixed. P_{avg} trends for three distinct connection performance goals. Without any material modifications, to see any improvement in RC delay, P_{avg} will have to be increased. Density targets (P_{eff}) must then be achieved by increasing the number of metal layers, although this strategy achieves an unfeasible amount of metal layers in only 1-3 generations, depending on the RC delay goal specified.

Reducing the dielectric constant and/or metal resistivity reduces the number of metal layers, but the impractical number is reached in just 1-3 generations if the RC delay is kept constant at 1.0x each generation. An even faster rise in the number of metal layers would result from a more aggressive RC delay improvement target. This emphasizes the vital significance of building better interconnects in order to keep ULSI density and performance trends going.

Changes in interconnect materials like Cu and low ε dielectrics will help a lot, but other improvements will be required as well. To minimize overdesign or unforeseen performance constraints, circuit designs must more correctly represent interconnect performance, and automatic layout techniques must make more efficient use of existing interconnects.

Novel ideas are essential for achieving better performance of interconnects at low cost in ultra-deep submicron ULSI circuits. Self-aligned quadruple patterning (SAQP) approaches for trenches and vias have been developed with better pattern. Large width metal lines for local interconnect length while preventing metal-to-via shorting are enabled by self-aligned interconnect features. A new approach that continues this trend is Directed Self-Assembly (DSA), which uses a looser pitch template printed in photoresist and block-copolymers that separate into micro-phases to generate the desired features. This

unique patterning technique needs process and circuit architectural co-optimization, similar to SAV-style optimization, to fully benefit from the self-alignment.

5. Conclusion

Transistor speeds have continued to rise as a result of pitch scaling and new process technology advancements. Today, interconnects account for a substantially bigger proportion of overall integrated circuit delay than in the past. This study compares interconnect and transistor scaling, analyses significant interconnect scaling problems, and emphasizes the necessity for transistor/interconnect co-optimization to build high-performance and high-yielding interconnects suitable for future ULSI requirements. The current trend of increasing interconnect RC latency while decreasing interconnect pitch will not meet future ULSI circuit performance needs. Increasing metal aspect ratios and adding more connection layers are two tactics for enhancing interconnect performance and density; however, these methods will hit their practical limits in a few generations. To overcome the growing limitation that interconnects pose to ULSI performance, new interconnect materials and enhanced circuit design methodologies will be required.

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