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Development and Study of 15 Level Multilevel Inverter for AC Distribution System in High Frequency Application

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***Abstract*: For high-frequency AC power distribution systems, this study introduces a new multilevel inverter topology. Compared to other existing multilevel inverter, the suggested technology produces a staircase waveform with a higher number of output voltage levels with higher frequency. In the proposed system, the total number of switches and sources that used are extremely low. The harmonic content of the output voltage waveform is reduced as the number of levels increases. The type of multilevel inverter used in this paper is a cascaded multilevel inverter. To maximize the number of voltage levels, H-bridge configuration is proposed with three asymmetrical voltage sources as input with three diodes for construction. The output of the proposed topology can generate 15-level high-frequency voltage waveforms.**

***Keywords*: multilevel inverter, diode, THD.**

1. Introduction

Multilevel inverters have procured significant traction in recent years as a result of their high operational capacity, minimal switching losses, and increased efficiency [1], [2]. With the primary idea of the Three-level Multilevel Inverter [3], [4], Nabe et al., first introduced the name 'Multilevel Inverter' in 1981. Multilevel inverters are picking up notoriety due to their capacity to handle the developing require for tall control evaluated applications, as well as the made strides control quality related with lower add up to consonant twisting. Multilevel inverters (MLIs) are well-established and broadly utilized control converters for medium to large-scale control supply [5]. The MLI has several advantages, including low dv/dt stress and low total harmonic distortion (THD) [6]. Traditional technologies are better suited to a variety of high voltage and high-power applications, but they have low dv/dt stress and a high number of switches, diodes, and dc-link capacitors or dc sources [7], [8]. New MLI topologies use fewer power switches and stress level is also low. However, while these topologies reduce the number of switches, they result in high dv/dt stress. In addition, new MLIs are used in this project [9] to reduce the load on switches and the number of switches. This MLI topology is better for producing high voltage levels with fewer switches. Multiple voltage sources are combined in multilayer inverters to produce a stepped waveform. The waveform becomes closer to a sinusoid as the number of steps is increased, diminishing harmonic content [10].

2. Multilevel Inverter Topology

In MLIs, there are three different kinds of topologies i.e., Diode clamped, Flying Capacitor, and Cascaded Multilevel Inverter. A diode that transferring a restricted amount of voltage in diode are called diode clamped MLI, which can decrease the burden on other electrical devices and a capacitor, which provides a DC offset from the stored charge. The flying capacitor multilevel converter may be a as of late created converter topology guaranteeing an adaptable control and secluded plan. In any case, the flying capacitor multilevel converter requires a adjusted DC voltage dissemination. Cascaded multilevel inverters are based on a arrangement association of a few single-phase inverters. This structure is able of coming to medium yield voltage levels utilizing as it were. standard low voltage develops innovation components. Cascaded H-bridge based on current-source inverter (CSI) is a developing control topology that employments a current-source inverter and a capacitive channel to synthetize a controlled voltage source that can be associated in arrangement with other controlled voltage sources in arrange to reach higher voltage levels.

A. Research Gap

- Development of a novel multilevel inverter circuit without switched capacitor with fewer switches not provided.
- Mathematical derivation is not provided for design the multilevel inverter circuit.
- Total number of switches are not minimized.

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- High frequency ac output for different types of loads is not provided to calculate the THD.
- THD mathematical calculation not provided.

B. Contributions

The contributions of the novelist to this work are as follows:

- Complete numerical condition given for novel planning of multilevel inverter circuit.
- Less number of switches are utilized in proposed topology.
- It is used for different types of loads with high frequency.
- Mathematical calculation of THD explain systematically.

C. Novelty of Proposed System

- The proposed framework can be able to produce 15-Level high frequency ac output with different types of loads.
- The proposed framework employments with seven switches to deliver 15-Level ac output.

3. Block Diagram of Proposed Topology

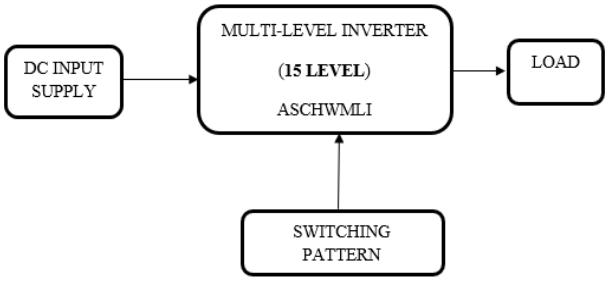

Fig 1. Complete proposed block diagram

The proposed block diagram in fig. 1 is clarified as follows:

- DC supply as input given to the multilevel inverter.
- Cascaded H bridge asymmetrical multilevel inverter associated to load.
- Switching pulse is given to the multilevel inverter through pulse generator circuit.
- The multilevel inverter will Produce high frequency 15 level AC output at load side.

4. MATLAB Simulation of R-load

The suggested multilayer inverter has fewer switches than previous models. Three MOSFET as switches (s1, s2, s3) are linked in series across the DC side and three asymmetrical voltage sources (V1=6V, V2=12V, V3=24V) with three diodes in parallel for unidirectional current flow, and a R load is connected parallel to switches. On the inverter side, four MOSFET as switches (s4, s5, s6, s7) are connected in an H-Bridge configuration, with a R load connected in parallel. The load is connected to a scope, which displays a 15-Level output waveform. The scope of a voltmeter and an ammeter is to measure voltage and current in an output waveform. It is shown in fig 2 and Circuit diagram is in Fig. 3.

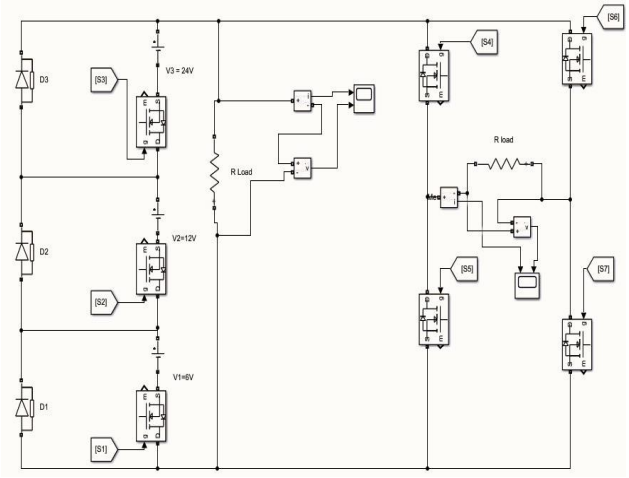

Fig. 2. 15-level MLI with R-load

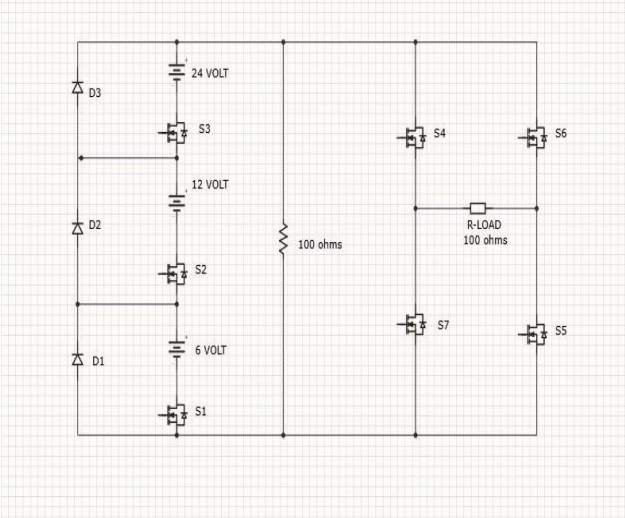

Fig. 3. Circuit diagram of 15 level with R-load

5. Circuit Diagram of 15-level MLI with R-load

A. Modes of Operation

At V1=6V, V2=12V, V3=24V

Mode 1 operation:

- For 0V, only S4, S7On, All other Switches OFF.

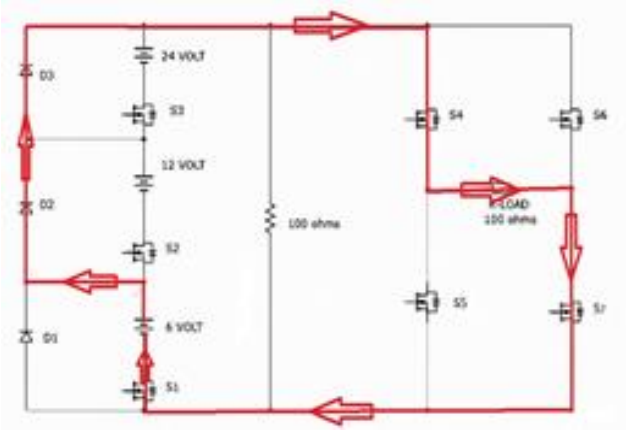

Fig. 4. Modes of operation for 6V for positive half cycle

Mode 2 operation:

- At 6V, for Positive half cycle, Switches S1, S4, S5 are turned ON
- For Negative half cycle, Switches S1, S6, S7 turned ON. It is shown in Fig. 4 & Fig. 5.

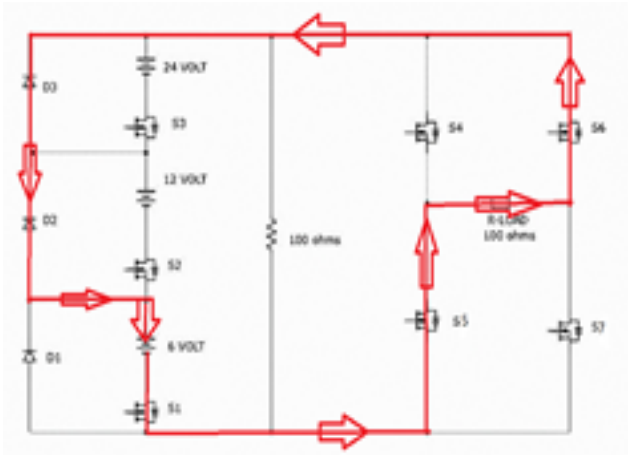

Fig. 5. Modes of operation for 6V for negative half cycle

6. MATLAB Simulation of RL Load

The suggested multilayer inverter has fewer switches than previous models. Three MOSFET as switches (s1, s2, s3) are linked in series across the DC side and three asymmetrical voltage sources (V1=6V, V2=12V, V3=24V) with three diodes in parallel for unidirectional current flow, and a RL load is connected parallel to switches. On the inverter side, four MOSFET as switches (s4, s5, s6, s7) are connected in an H-Bridge configuration, with a RL load connected in parallel. The load is connected to a scope, which displays a 15-Level output waveform. A scope is attached with load to display 15-Level output waveform. A voltmeter and ammeter relate to scope to measure the voltage and current in output waveform. It is shown in Fig. 6 & Fig. 7.

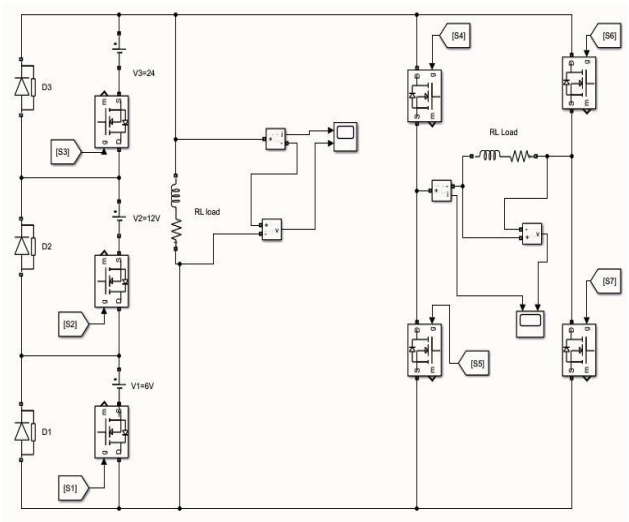

Fig. 6. 15-level inverter circuit with RL load

7. Circuit Diagram of 15 Level MLI with RL-load

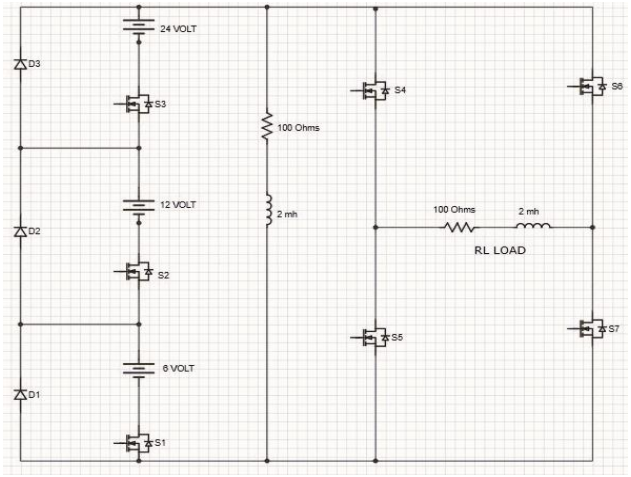

Fig. 7. Circuit diagram of 15 level with R-load

8. Results and Discussion

The proposed 15-level MLI is simulated using MATLAB/Simulink. For the same specifications, the simulation output for R-load with V1=6V, V2=12V, V3=24V AT F=1000 Hz, 2000 Hz, 3000 Hz, 4000 Hz, and 5000 Hz is shown in Fig. 8, Fig. 10, Fig. 12, Fig. 14 & Fig. 16. The FFT analysis is shown in Fig. 9, Fig. 11, Fig. 13, Fig. 15 & Fig. 17.

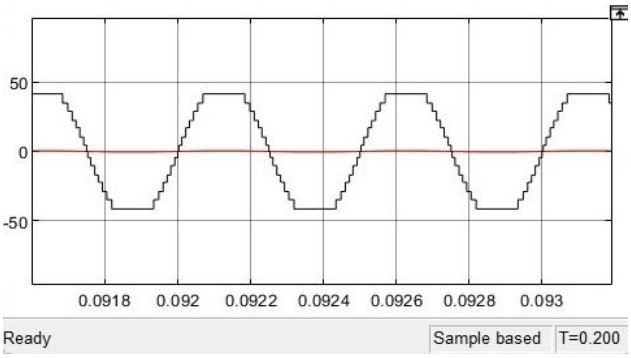

Fig. 8. Simulation output of R load at 1000Hz (42V)

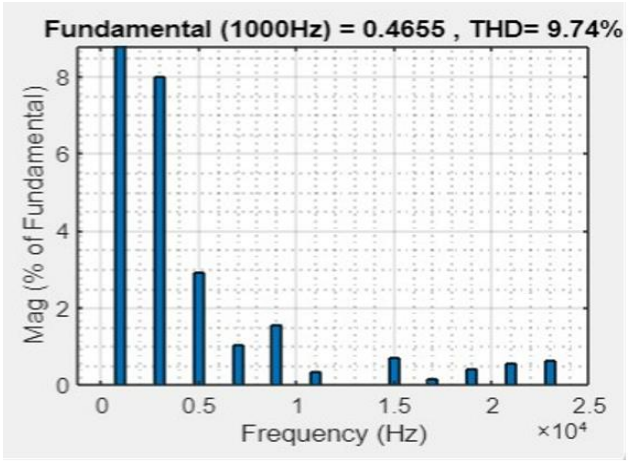

Fig. 9. FFT analysis of R load at 1000Hz(42V)

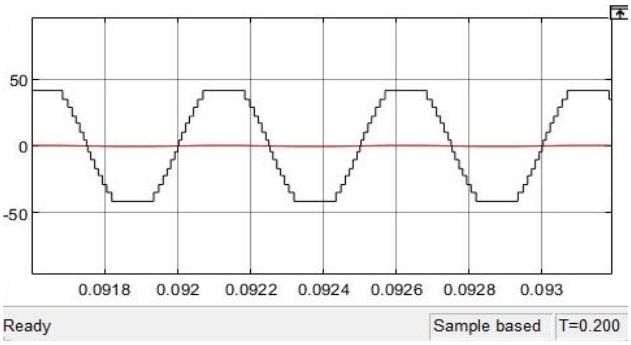

Fig. 10. Simulation output of R load at 2000Hz(42V)

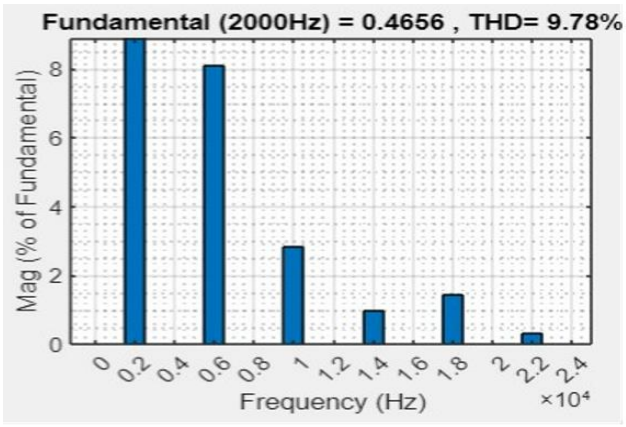

Fig. 11. FFT analysis of R-load with 2000 Hz(42V)

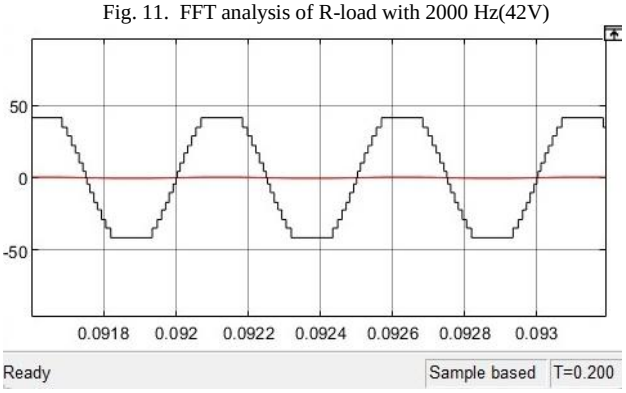

Fig. 12. Simulation output of R load at 3000Hz(42V)

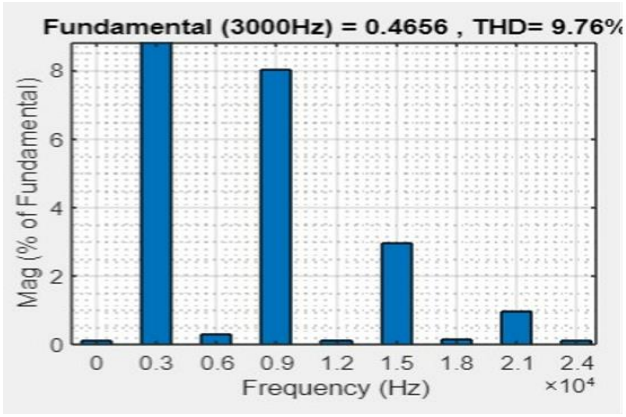

Fig. 13. FFT analysis of R-load with 3000 Hz (42V)

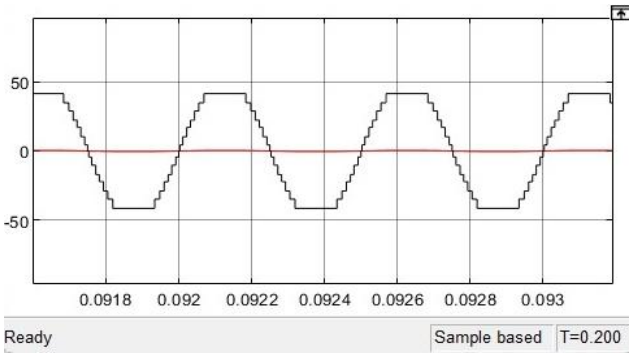

Fig. 14. Simulation output of R load at 4000Hz (42V)

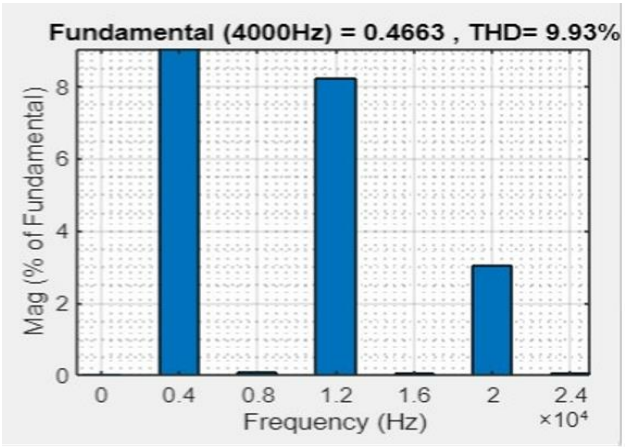

Fig. 15. FFT analysis of R load at 4000Hz (42V)

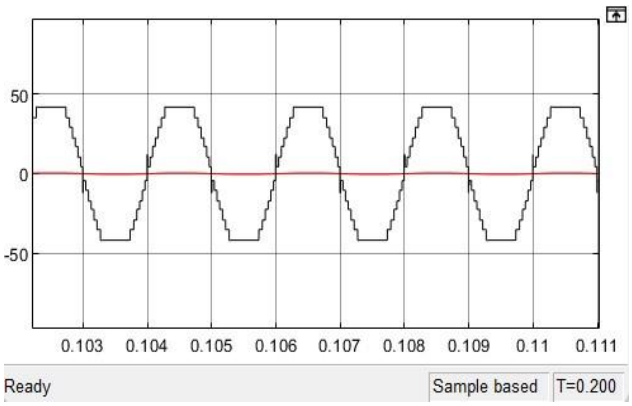

Fig. 16. Simulation output of R load at 5000Hz (42V)

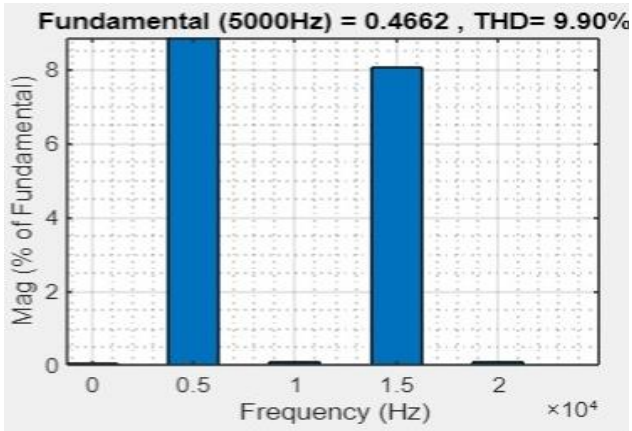

Fig. 17. FFT Analysis of R load at 5000Hz (42V)

Similarly, the proposed 15-level MLI is simulated using MATLAB/Simulink for the similar specifications. The simulation output for RL-load with V1=6V, V2=12V, V3=24V AT F=1000 Hz, 2000 Hz, 3000 Hz, 4000 Hz & 5000 Hz is shown in Fig: 18, Fig 20, Fig: 22, Fig: 24 & Fig: 26. The FFT analysis is shown in the Fig: 19. Fig: 21, Fig: 23, Fig: 25 & Fig: 27.

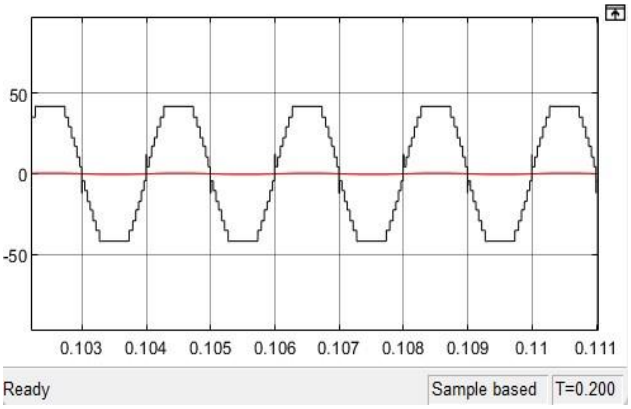

Fig. 18. Simulation output of RL load at 1000Hz (42V)

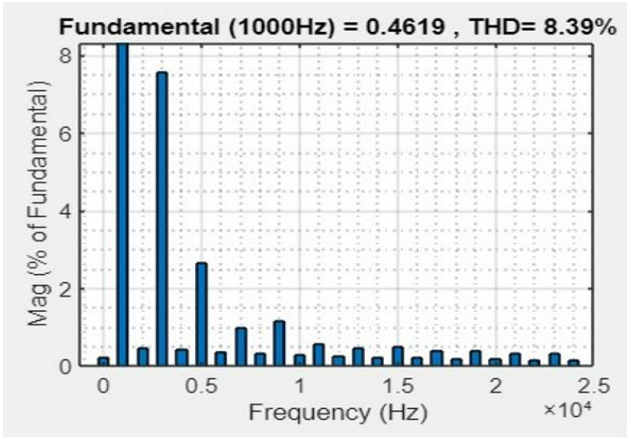

Fig. 19. FFT analysis of RL-load with 1000 Hz (42V)

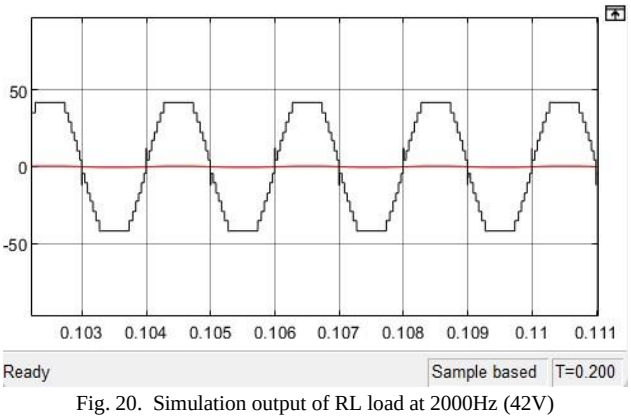

Fig. 20. Simulation output of RL load at 2000Hz (42V)

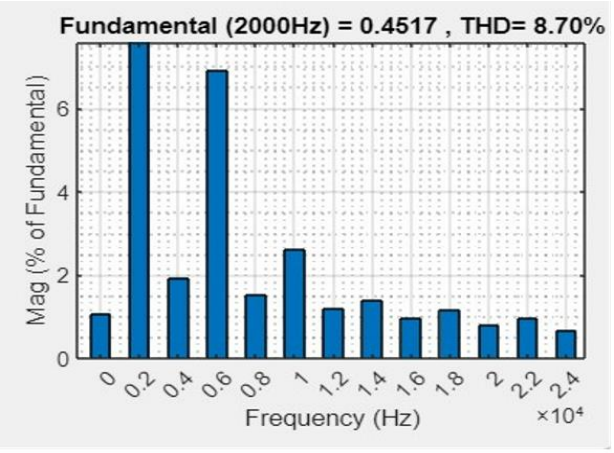

Fig. 21. FFT analysis of RL load at 2000Hz (42V)

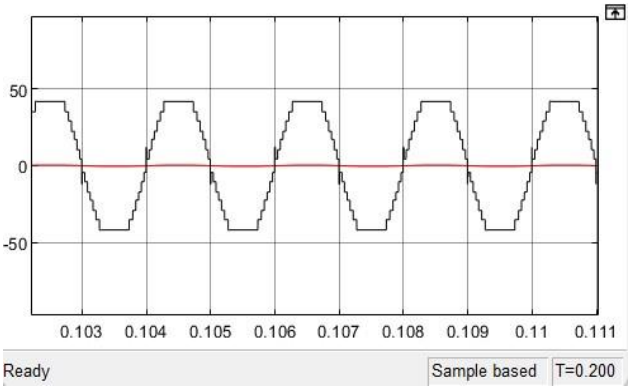

Fig. 22. Simulation output of RL load at 3000Hz (42V)

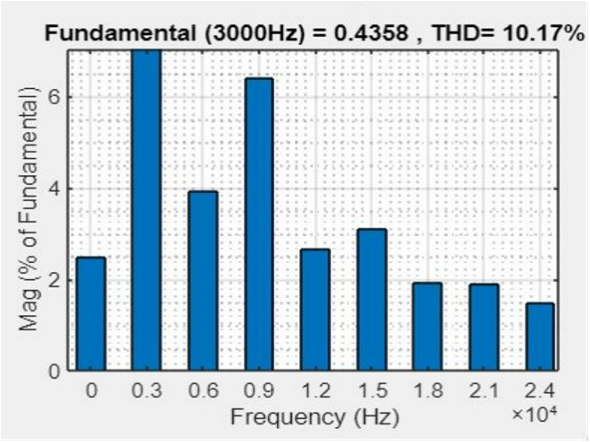

Fig. 23. FFT analysis of RL load at 3000Hz (42V)

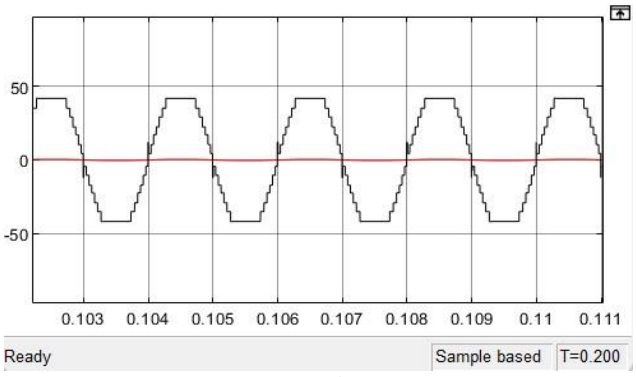

Fig. 24. Simulation output of RL load at 4000Hz (42V)

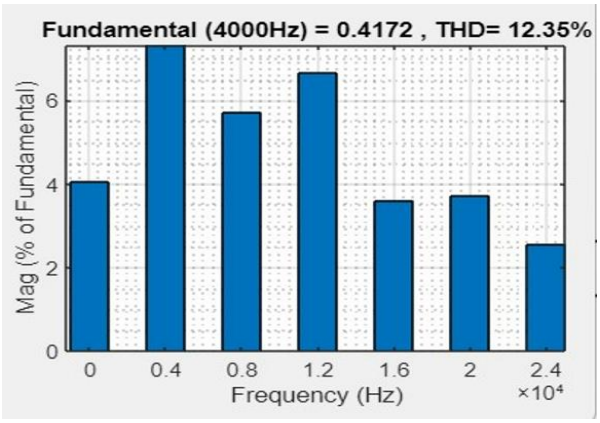

Fig. 25. FFT analysis of RL load at 4000Hz (42V)

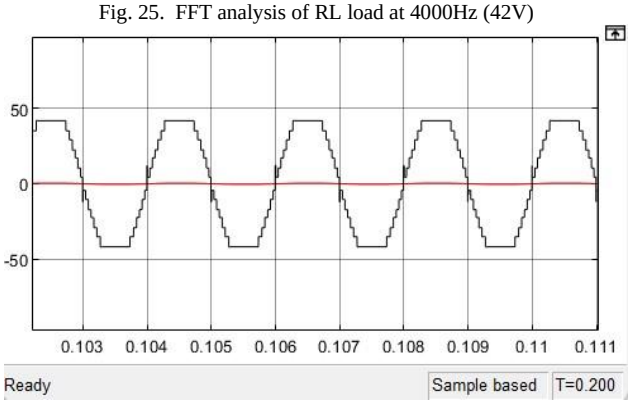

Fig. 26. Simulation output of RL load at 5000Hz (42V)

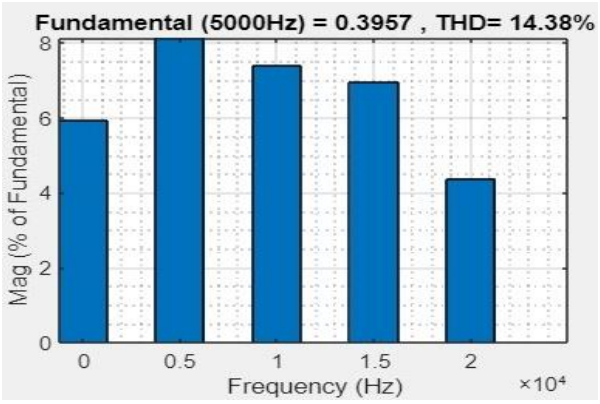

Fig. 27. FFT analysis of RL load at 5000Hz (42V)

Table 1
Result analysis with R-load

Input voltage(V)	Output Voltage(V)	Current (A)	Frequency (Hz)	Simulated THD(%)	Calculated THD(%)	Power (W) V X I X PF
V1=6V V2=12V V3=24V	VOut=42V	I=0.8A	F1=1000	9.74%	10.03%	42X0.8X1 =33.6 W
			F2=2000	9.78%	10.14%	
			F3=3000	9.76%	10.00%	
			F4=4000	9.93%	10.00%	
			F5=5000	9.90%	10.00%	

Table 2
Result analysis with RL-load

Input voltage(V)	Output Voltage(V)	Current (A)	Frequency (Hz)	Simulated THD(%)	Calculated THD(%)	Power (W) V X I X PF
V1=6V V2=12V V3=24V	VOut=42V	I=0.9A	F1=1000	8.39%	8.50%	42X0.9X 0.707 =26.72 W
			F2=2000	8.70%	8.95%	
			F3=3000	10.17%	10.57%	
			F4=4000	12.35%	13.43%	
			F5=5000	14.38%	14.28%	

9. Conclusion

A novel cascaded H-Bridge multilevel inverter has been proposed. In MATLAB Simulink, a 15-level circuit topology is examined in detail. Comparing to a routine CMI, the suggested inverter can reduction the number of switches. As the number of voltage levels develops exponentially, and the harmonics within the staircase output are altogether decreased, which is especially impressive due to basic and flexible circuit topology. As a result, the recommended multilevel inverter can be used to generate HF power with a controllable magnitude and less harmonics.

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