International Journal of Recent Advances in Multidisciplinary Topics
Volume 4, Issue 5, May 2023
https://www.ijramt.com | ISSN (Online): 2582-7839

Performance Analysis of Multi Operand Adders

Laxmi Pardhi[1*], Sharda Mungale[2]
[1]Student, Department of Electronics Engineering, Priyadarshini College of Engineering, Nagpur, India
[2]Assistant Professor, Department of Electronics Engineering, Priyadarshini College of Engineering, Nagpur, India

***Abstract*: In this paper, Ripple carry adder and Wallace tree adder is designed, encoded in Verilog, and simulated in Xilinx software. This paper presents the pertinent choice for selecting the adder topology with the tradeoff between delay, power consumption and area.**

***Keywords*: Ripple carry adder, Wallace tree adder.**

1. Introduction

Multi-operand adders usually consist of compression trees which reduced the number of operands per a bit to two, and a carry-propagate for the two operands in ASIC implementation. A method to compute the exact number of carry bits required for a multi-operand addition operation. A fast combinatorial parallel 4-operand adder module is presented. The area, delay and energy efficiency of the BTA depends on the performance of adders. Which can be used to develop the BTA structure, where each adder has its own tradeoffs between area, delay and energy consumption. In this work, the following adder structures are used: Ripple Carry Adder and Wallace Tree Adder.

A. Ripple Carry Adder (RCA)

The ripple carry adder is constructed by cascading full adders (FA) blocks in series. One full adder is responsible for the addition of two binary digits at anystage of the ripple carry. The carryout of one stage is fed directly to the carry-in of the next stage. Even though this is a simple adder and can be used to add unrestricted bit length numbers, it is however not very efficient when large bit numbers are used. One of the most serious drawbacks of this adder is that the delay increases linearly with the bit length. The worst-case delay of the RCA is when a carry signal transition ripples through all stages of adder chain from the least significant bit to the most significant bit, which is approximated by:

$$t = (n - 1)\, t_c + t_s \qquad (1)$$

Where t_c is the delay through the carry stage of a full adder, and t_s is the delay to compute the sum of the last stage. The delay of ripple carry adder is linearly proportional to n, the number of bits, therefore the performance of the RCA is limited when n grows bigger. The advantages of the RCA are lower power consumption as well as compact layout giving a smaller chip area. The design schematic of RCA is shown in figure 1.

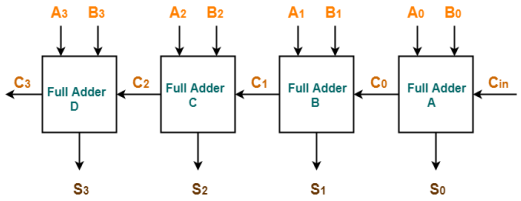

Fig. 1. 4-bit ripple carry adder

The Wallace tree adder is a type of digital circuit used for high-speed arithmetic computations in computers and other electronic devices. It is designed to perform the addition of two binary numbers with minimum delay and a reduced number of partial sum bits compared to other types of adders.

The Wallace tree adder circuit consists of three main components: a half-adder circuit, a full-adder circuit, and a tree structure of multiple full-adders. The half-adder circuit takes two single-bit inputs and produces a single-bit sum and a carry bit output. The full-adder circuit takes three single-bit inputs (two operands and a carry-in bit) and produces a single-bit sum and a carry-out bit output.

The Wallace tree adder works by breaking down the two input numbers into groups of three bits each and performing a series of additions and carry propagations in a tree structure. Each group of three bits is processed by a full-adder circuit, which produces two outputs: a two-bit partial sum and a one-bit partial carry. These outputs are then combined in pairs using another layer of full adders to produce the next level of partial sums and carries.

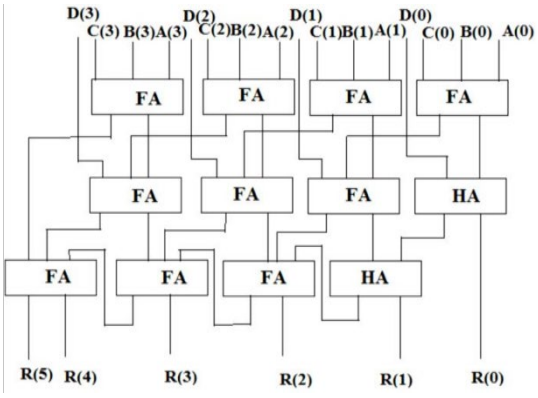

Fig. 2.

*Corresponding author: laxmipardhi08@gmail.com

This process continues recursively until the final output is obtained, which is a single binary number representing the sum of the two input numbers. The final carry-out bit, if any, can be discarded as it does not contribute to the sum.

The Wallace tree adder circuit is highly efficient in terms of speed and area usage compared to other types of adders, making it a popular choice for high-performance computing applications. However, it requires a significant amount of circuitry and is more complex to design and implement than simpler adders such as the ripple carry adder.

The simulation and synthesis is done on these two adders.

RTL view of 16-bit Ripple Carry Adder

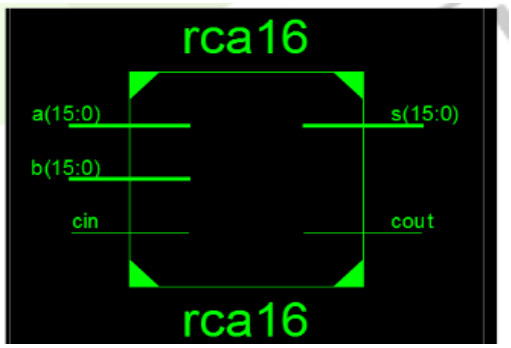

Fig. 3. 16-bit Ripple Carry Adder (RCA) RTL Diagram

As shown in figure 3, 16-bit ripple carry adder diagram using VHDL/Verilog Coding is implemented in Xilinx Software ISE 12.2i. Full adder vhdl/Verilog coding synthesized with Register Transfer Level (RTL) diagram and Technology RTL is synthesized, post and route generated as shown in Figure 3, 4 and simulated full adder output waveform a[15:0]=16'hABCD, b[15:0]=16'hABCD and cin=1'b0 then sum[15:0]=16'h579a, c_{out}=1'b1 else a[15:0]=16'h1A2D, b[15:0]=16'hBC66 and c_{in} =1'b1 then sum[15:0]=16'hD694,cout=1'b0 as shown in Figure 5 and generate bit file to fused in Xilinx PROM XCF32p and implemented in FPGA.

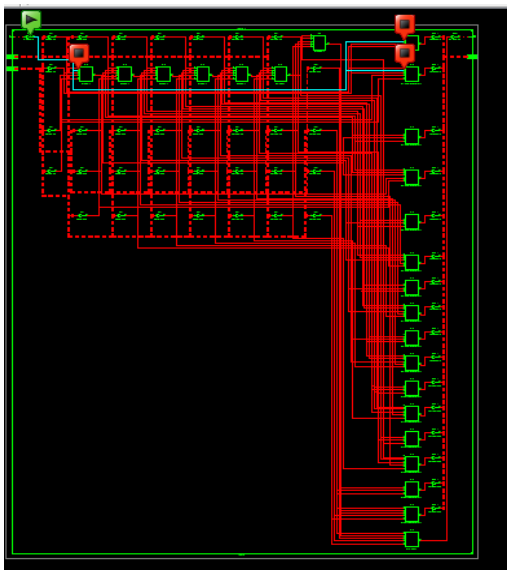

Fig. 4. 16-bit Ripple Carry Adder (RCA) Technology RTL diagram

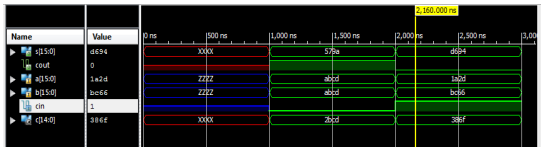

Fig. 5. 16-bit Ripple Carry Adder (RCA) timing diagram

2. Result

Table 1
Comparison of RCA and WTA in terms of AREA

AREA	RCA (μm²)	WTA (μm²)
4-bit	936	772
8-bit	2376	1620
16-bit	4248	3213

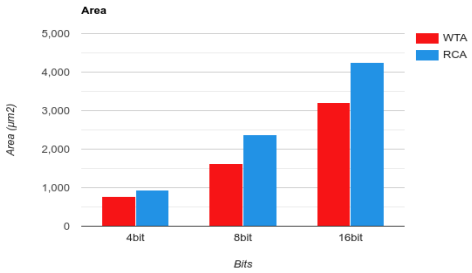

Fig. 6.

Table 2
Comparison of RCA and WTA in terms of POWER

POWER	RCA (μw)	WTA (μw)
4-bit	153.9	133.68
8-bit	483	315.23
16-bit	711	689.30

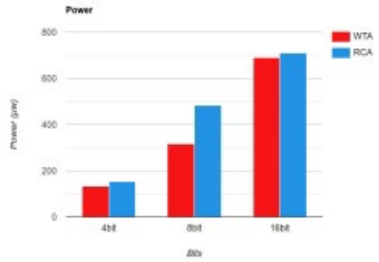

Fig. 7.

Table 3
Comparison of RCA and WTA in terms of DELAY

DELAY	RCA (ns)	WTA (ns)
4-bit	8.95	3.475
8-bit	13.20	6.574
16-bit	28.74	8.866

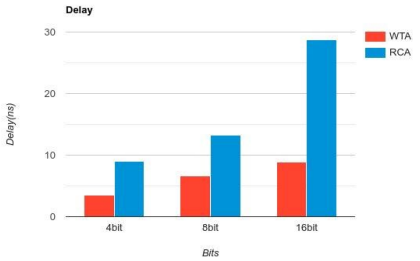

Fig. 8.

3. Conclusion

In this manuscript, it has been discussed the high performance Ripple Carry Adders (RCAs) in digital logic circuits design with uses of Addition forms the basis for many processing operations, from ALUs to address generation to multiplication to filtering. As a result, adder circuits that add two binary numbers are of great interest to digital system designers. An extensive, almost endless, assortment of adder architectures serves different speed/power/area requirements. This section begins with half adders and full adders for single-bit addition. It then considers a of ripple carry adders (RCAs) for the addition of multi bit words in digital logic design and systems. In addition, with Testing of RCAs 32, 64-bit adder's waveform generation using Mentor Graphics Tool Model Sim. And compare different digital words bit like 4, 8, and 16bit in the performance of device area and timing analysis using Xilinx FPGA.

References

[1] Sujit Patil, Subodh Kumar Singhal, "Area Delay and Energy Efficient Multi Operand Binary Tree Adder", June 2020.

[2] Rajwinder Kaur, Amit Grover, Vishal Sharma, "An Efficient Carry Select Adder Design by using different Topologies" July2015.

[3] Sakshi Sharma, Pallavi Thakur, "Design of High-Speed Power Efficient Wallace Tree Adders", May 2016.

[4] R.UMA, Vidya Vijayan, M. Mohanpriya, Sharon Paul, "Area, delay and power comparison of adder topologies", February 2012.

[5] S. Archana, G. Durga "Design of Low Power and High-Speed Ripple Carry Adder", 2014.

[6] Kokila Bharti Jaiswal, Nithish Kumar V., Pavithra Seshadri and Lakshminarayanan G., "Low Power Wallace Tree Multiplier Using Modified Full Adder", 2015.

[7] D. Thabah, M. Sonowal and P. Saha, "Experimental Studies on Multi-Operand Adders", International Journal of Applied Engineering Research, vol. 12, no. 13, pp. 3665-3670, 2017.

[8] K. Rajesh and G. Umamaheswara Reddy, "FPGA Implementation of Ripple Carry and Carry Look Ahead Adders Using Reversible Logic Gates", International Journal of Applied Engineering Research, vol. 12, no. 13, pp. 3665-3670, 2017.

[9] Aritra Mitra, Amit Bakshi, Bhavesh Sharma, Nilesh Didwania, "Design of a High-Speed Adder," International Journal of Scientific & Engineering Research, vol. 6, no. 4, April 2015.

[10] S. Yuvaraj, K. K. Senthilkumar, K. Senthamil Selvan, A. R. Aravind, "High Performance Ripple Carry Adders in VLSI Design," in International Journal of Creative Research Thoughts, vol. 10, no. 6, June 2022.