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A Compact 30-GHz 18-dBm Power Amplifier for 5G Communication in 180-nm CMOS

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***Abstract*: Currently, there is a large move towards 5G wireless technology beyond the existing, widely used 4G technology due to an increased use of smart devices, and multimedia content. 5G technology is expected to operate at high frequencies between 1 GHz to 100 GHz opening up a new horizon for spectrum constrained future wireless communications. Designing high efficiency power amplifiers for such high frequencies presents a new challenge. This project designs an efficient Stacked Power Amplifier (PA) for 5G. The power amplifier is implemented in 180nm technology using LT spice tool. The usage of a diode pre-distorter for analog pre- distortion is investigated for the stacked Power amplifier design. It is shown, that the linearity of the stacked PA is significantly improved compared to a bipolar transistor at almost no additional layout size. This paper presents design of a 30 GHz power amplifier for fifth- generation (5G) mobile communication in CMOS design. The stacked power amplifier consists of two different stages of architecture. With 5-V supply, the stacked power amplifier achieves a small-signal gain of 16 dB, saturated output power (Psat) of 18 dBm, and achieves the maximum power added efficiency of 34.79%. The amplifier has been designed in 180-nm CMOS.**

***Keywords*: Analog pre-distortion, Power amplifier, Power added Efficiency, Frequency, 5G.**

1. Mobile Communication

Due to the numbers of users and great demand in downloading and uploading content there has been a extreme increase in the use of smart phones in the recent years. Since mobile users are expecting more data speed and secure service for the current 4g technology, these 4g cannot be supported. This technology will impact following mobile communications system,

- 100x more storage
- Higher data speed
- Higher Frequency
- High service providers

Due to usage of high data used by the current users, the service providers have a problem with the current RF band. To overcome this 5G technologies will provide a new spectrum that has not been used before. Since 4G networks operates at less GHz downloading and uploading data is lower. To overcome this 5G technology is expected to operate at a frequency of more than 100GHz. The millimeter wave spectrum shows the possible of giving thousands of times of more data in a future wireless communication [2]. The large amount of power in the transmitter are being consumed by the power amplifier. Due to limited efficiency and dynamic range in the power amplifier, high power is consumed and the power amplifier gives a linear behavior [1]. 5G applications are studied because of their low cost and functionality. 5G technology for recent years shown the need for highly linear and effective power amplifier in order to give high data rate [4]. More CMOS design is possible in order to control the power output drawn on the current and the circuit voltage. In addition, output power needs linearity circuit.

In wireless communication systems Power amplifier (PA) plays a major role in it. The power amplifier output power required is as high as possible for a Long Communication Systems. Due to less breakdown voltage, the power amplifier in CMOS has low saturated output power. To improve the power amplifier status, transformer based differential design for output sequence is preferred. In this paper, 30-GHz CMOS power amplifier design and theoretical values are presented. The improved design and waves for high frequency and high power added efficiency are given. The simulation results the large signal performance and small signal gain results.

The remaining paper is organized as follows. Part 2.0 describes existing works on stacked power amplifier identification. Part 3.0 presents the circuit designs and analysis of AC and DC power sources. Part 4.0 reports the analytical and theoretical values of the circuit. Part 5.0 discusses the significance of the observed findings. Part 6.0 concludes this paper.

2. Related Work

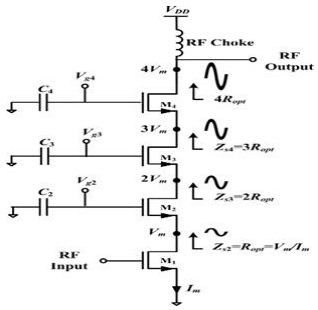

Fig. 1. Stacked power amplifier

In wireless communication system, Power amplifier plays an important role in it. There are different types of power

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amplifiers among, stacked power amplifier is one of the technologies which has high gain and frequency. Stacked technique is nothing but series of transistors are arranged, with input are given in the one end and output are taken by the other end. Capacitance acts a rectifying element to this stacked power amplifier. It isolates the input signal and biasing voltage. Since the input signal is applied to this transistor via this coupling transistors. The uses of power amplifier are, it increases the high input power level and produce the required output power. In multi cell stacked devices this series input configuration plays an important role. In base station the RF power signals are boosted by this power amplifier. It was based on two technologies; one is silicon based and another one is Diffused Metal oxide semiconductor or RF gallium nitride. Generally, the 3G base stations are based on LDMOS. These LDMOS are highly inexpensive due to this they took nearly a year to implement in 4G. In base stations these power amplifiers play an important role in converting a lower power RF signals into a very high-power signal. In the base station not only the power amplifier used and there are many devices based on their various process.

1) Design parameters of power amplifier

There are certain parameters are designed to have an amplifier. To perform an amplifier in perfect way there are some parameters which are described below.

2) Gain

"Amplification" of an amplifier is measured by the gain of an amplifier. For example, by using we can calculate the voltage gain, current gain, power gain how much increase in the amp of a signal. In addition, it is the ratio of output signal amplitude divide by the input signal amp and it denotes by the symbol of "A". The gain for three different power amplifiers is derived using correct formula:

Voltage gain (A_v) = amplitude (output volt) / input voltage Amp

$$Av = \frac{Vout}{Vin} \quad (1.1)$$

Current gain (A_i) = amplitude (output current) / input current Amp

$$Ai = \frac{Iout}{Iin} \quad (1.2)$$

Power gain (A_p) = output power signal/input power signal

$$Ap = \frac{Pout}{Pin} \quad (1.3)$$

The gain of the three different power amplifiers is derived.

3) Frequency response

For all frequencies, the power amplifiers have a different gain. For example, in radio frequency the designed power amplifier amplifies more frequency i.e. more than 100 KHz and not amplify less than 100 KHz for signal having less frequencies. While in audio frequency the designed power amplifier operates less than 30 KHz and not amplify more than 30 GHz for signals having higher frequencies. By seeing this that the amplifier has a particular frequency response, where to operate the frequencies at above or below and where the amplification is needed.

4) Bandwidth

Bandwidth of an amplifier is obtained from the frequency response curve. 'Band' refers to a frequency of which the gain of the amplifier. At the center bandwidth the gain of the power amplifier is considered as insufficient compared to outside gain. For example, Output voltage frequencies should be at least 0.9 times maximum when compared to output voltage for voltage bandwidth. Bandwidths are measured in certain parameters they are, (Hz, KHz, MHz, GHz). For power bandwidth output power frequencies ranges at least 0.6 times the maximum power output.

5) Input impedance

Here the word impedance refers to resisting or protesting something. For example, it opposes to AC current to flow. At zero Hertz the impedance acts as a resistance, but frequencies more than zero Hertz it does not acts a resistance. Input terminals between the input impedance respectively. The word 'effective' states that the impedance is not act as a resistance just that of what power amplifiers across the inputs (capacitors, resistors), and allow as the certain value of current that can able to pass in a given source and for a given source signal voltage which was operates at a certain frequency. Input impedance are also used by a different factor like amplifier gain, applied frequency and used feedback signal that are connected with the amplifier output.

6) Output impedance

In amplifier output impedance are not dependent on the components that are actually connected with an amplifier output. It is a "clear" impedance and for amplifier output terminals these are responsible for voltage signal to fall in, when more current drawn from the output voltage signal as same as the current drawn from an output terminal respectively.

7) Design implementation

In this paper, AC and DC analysis of stacked power amplifier techniques are designed and analyzed. Envelop Tracking (ET) is the first CMOS power amplifier which was designed and used in wireless communication transmitters in order to improve the power added efficiency and the signal gain. DC analysis of stacked amplifier is shown in fig.3. In DC analysis bipolar transistors are replaced with CMOS design and measured the input and output power and also attain the frequency of operation at 5GHz with power added efficiency of 34%. In AC analysis the power amplifier attains the overall signal gain of 18dB with output power saturated of dBm, and it operates at the frequency of 5GHz. This entire circuit design was using LT spice platform in 180 nm technology.

8) Pre-distortion

Basically, pre-distortion techniques have classified into two types, which was analog and digital [3]. Less than 20 GHz applications are used by digital pre-distortion. Because of this it operates at less frequency and power consumption is less when compared to analog pre-distortion. In digital pre-distortion large baseband bandwidth operates at high clock rate. Normally in power amplifiers the operating frequency and high data speed are attain only in analog pre-distortion. The designed proposed power amplifier carried out one biasing scheme i.e. diode pre- distorter which was nothing but an analog pre-distortion. By using diode pre-distorter, it produces higher output power with lower input terminals and also produce a

better linearity signal [4]. The word distortion is nothing but it denotes the shape of things. For example, audio signal is being represented by sound and video signal is being represented by images [6].

3. Circuit Design

1) AC analysis

In wireless communication, power amplifier plays an important role. Required output power is generated by increasing the input power level. In this paper, we have designed a stacked power amplifier using analog pre-distortion technique in CMOS to improve signal gain and the Power added efficiency of the amplifier.

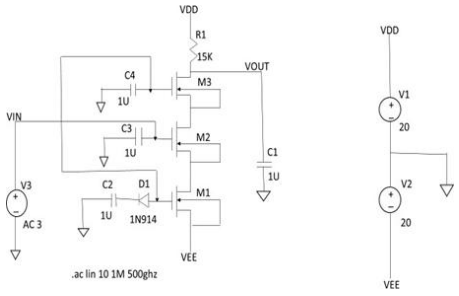

Fig. 2. Schematic of the proposed stacked power amplifier (AC Analysis)

Fig 2 Shows the circuit design of AC designed stacked power amplifier which was designed using LT spice platform in 180 nm technology. The input amplitude of this circuit is around 3V. The capacitor is connected in series to isolate the input signal and biasing voltage. The output of power amplifier normally driven by very low impedance network mostly consider as speaker, speaker is connected in the form capacitance c1 respectively. As the power increases in the input, the rectified dc current of the diode increases.

Gain-compression and phase distortion of circuit improves due to diode pre-distorter which acts as an analog pre-distortion. In this designed power amplifier, bipolar transistors are being replaced with CMOS design technique. It increases the power added efficiency. When we apply input signal to CMOS, it should not affect the biasing condition of CMOS, similarly the biasing voltage should not affect the input signal, to isolate the input signal and biasing voltage. Thus coupling capacitor is used, in other words, the input signal is applying to CMOS via this coupling capacitor in ac analysis. This designed power amplifier gives the overall the signal gain of greater than 16dB, and saturated output power pf 18dBm. This proposed design consumes less power, less heat generation and more stability as compared to bipolar transistor. This proposed stacked power amplifier operates between the frequencies of 30-GHz.

2) DC analysis

The proposed DC circuit design was shown in Fig: 3.2. In this design also bipolar transistors are replaced with MOS transistors. The bias networks are used as MOS transistors in order to improve the signal and power added efficiency.

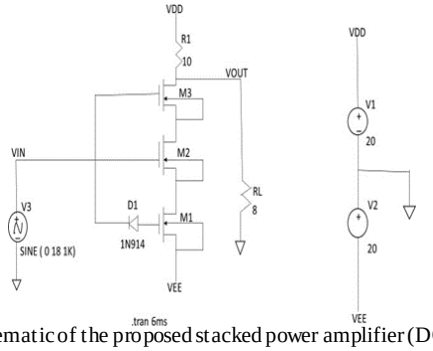

Fig. 3. Schematic of the proposed stacked power amplifier (DC Analysis)

Fig 3 Shows the Schematic of the DC designed stacked power amplifier, which was designed using LTSPICE platform in 180 nm technology. In this design the dual power supply is connected, due to this that the output swing is almost doubled [2]. We have given the sinusoidal input and the sine wave amplitude that is input amplitude around 18V and frequency around 1k and the output of the power amplifier is normally driven by the very low impedance network [5]. Mostly let's consider output load might be a speaker, so speaker is represented in the form of resistance [RL] over here.

4. Design and Analysis

1) AC equivalent model

For AC signal these capacitor acts as a short circuit. In this small signal equivalent model for CMOS, first consider all the dc sources as zero and replace the coupling and bypass capacitor with short circuit. Fig 4 shows the AC equivalent circuit of stacked power amplifier. As you aware the capacitor blocks dc signal, because for dc signal it will act as an open circuit. The operating frequency of capacitor for dc voltage is zero and the reactants of capacitor is infinity.

2) Voltage gain of the circuit

"Amplification" of an amplifier is measured by the gain of an amplifier. For example, by using we can calculate the voltage gain, current gain, power gain how much increase in the amplitude of a signal". From the above AC equivalent circuit, the voltage gain of circuit is derived below

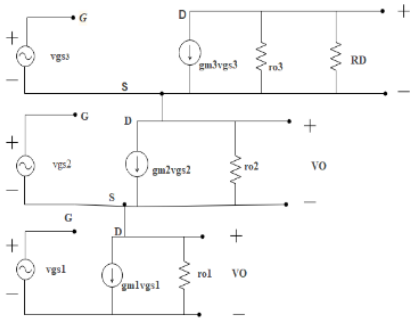

Fig. 4. AC equivalent circuit of proposed stacked power Amplifier

$V_{01} = -g_{m1}V_{gs1}$ (V_{gs1} is equal to v_i) $V_{01} = -g_{m1}$ (vi) **(4.1)**

$V_{02} = -g_{m2}V_{gs2}$ (V_{gs2} is

equal to v_i) $V_{02} = - g_{m2}$

(vi) **(4.2)**

$V_{03}/R - V_{02}/R - V_{01}/R + g_{m2} V_{gs2}$

$+ g_{m1} V_{gs1} = 0$ $V_{03}/R - V_{02}/R =$

$V_{01}/R + g_{m2} V_{gs2} + g_{m1} V_{gs1} = 0$

$V_{03}/R = 1/R + g_{m2} (-g_{m1}(vi) +$

$g_{m1} V_{gs1} + V_{02})$ $V_{03}/R = - g_{m1} r$

(g_{m2})

$A_v = - (g_{m1} r) (g_{m2} r) (g_{m3} r)$ **(4.3)**

This result can be derived from the m1.m2, m3 changes an input voltage ΔV_{in} to a drain current change $(g_{m1})(g_{m2})(g_{m3})$ ΔV_{in} and hence an output voltage change $- (g_{m1})(g_{m2})(g_{m3}) R$ $\Delta V_{in.}$ Since g_m itself varies with the input signal according to $g_m = \mu_n C_{ox} (w/l) (V_{GS} - V_{TH})$, If the signal is large, then the gain of the circuit changes significantly.

3) Input impedance

At low frequencies the input impedance (Im) of the proposed circuit is at peak. M3 is off when the input voltage increases from zero and Vout= VDD. As Vin approaches VTH, when M3 turns on it draws current from R and it lowers the Vout respectively. If VDD is not excessively low, M3 turns on in saturation, and we have

Reference	This study	[1]	[2]	[3]	[4]
Technology	180 nm CMOS	130 nm CMOS	180 nm CMOS	130 nmSiGe	60 nm CMOS
Frequency(GHZ)	30	28	2.8	24	32
PAE(max) %	34.79	26	25.54	35	32.9
(Psat)power(dBm)	18	16	7.05	18.6	15.3
Gain (dB)	16	14.6	7.17	15	12.9
Vdd(v)	5	5.5	5	4	1.1

$$V_{out} = V_{DD} - R \tfrac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH})^2 \quad (4.4)$$

When Vin increases the channel length modulation is neglected and Vout drops high and in saturation point the transistor continues to operate until Vin exceed Vout and by Vth.

$$V_{out} = V_{DD} - R \tfrac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH})^2 \quad (4.4)$$

When Vin increases the channel length modulation is neglected and Vout drops high and in saturation point the transistor continues to operate until Vin exceed Vout and by Vth.

$$V_{in3} - V_{TH} = V_{DD} - R\tfrac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{TH})^2 \quad (4.5)$$

From which $V_{in1} - V_{TH}$ and hence V_{out} can be calculated

for $V_{in} > V_{in3}$, m3 is in triode region

$$V_{out} = V_{DD} - R\tfrac{1}{2}\mu_n C_{ox} \frac{W}{L} 2(V_{in} - V_{TH}) V_{out} - V_{out}^2) \quad (4.6)$$

$V_{out} << 2 (V_{in} - V_{TH})$, and from the equivalent circuit of figure .4.1

$$V_{out} = V_{DD} \frac{R}{R + r_p}$$

$$V_{out} = V_{DD}/1 + \mu_n C_{ox} \frac{W}{L} R (V_{in} - V_{TH}) \quad (4.7)$$

4) Trans conductance of the circuit

$$ID = \frac{\mu C_{ox}}{2} \frac{W}{L} / 1 (VGS - Vt)$$

$$Gm = \partial ID / \partial VGS = \frac{2\mu C_{ox}}{2} \frac{W}{L} / 1 (VGS - Vt)$$

$$Gm = \mu n Cox(w/l) (VGS - Vt)$$

$$Gm = 2ID / VGS - VT \quad (4.8)$$

5) Theoretical value

Theoretical value of the voltage gains achieved 16dB, 18 dBm Bandwidth (BW) 30- GHz (80%) with 18dBm of maximum Saturated output power and with maximum power added efficiency of 34.86%.

5. Calculations

1) Input DC power

Pin (DC) = VCC X ICQ

= 40 x (1.111/3.14)

= 14.14W

2) Output AC power

Pout (AC) = vorms x iorms

= 8.88 x (1.11 x 0.5)

= 4.92

3) Power added efficiency

$$\%efficiency = 100 \times [pout^{(ac)} / pin\ (dc)]$$

$$= 100 \times [4.92w / 14.14W]$$

$$= 34.79\%$$

6. Simulation Results

Fig 5 Shows the AC analysis of stacked power amplifier, which was simulated using LT spice tool in 180 nm technology. Presenting good input matching and gives the small signal gain of 16 dB, this stacked power amplifier shows a measured (Psat) power of 18 dBm, frequency at 30- GHz and with maximum power added efficiency of 34.86%.

Table 1

Performance comparison with various power amplifiers for 5G CMOS

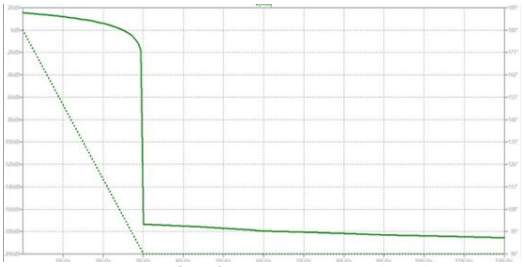

Fig. 5. Simulated Frequency-Freq. (GHz)

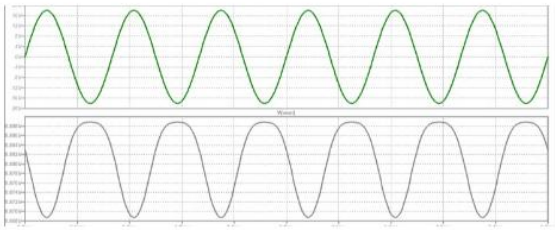

Fig. 6. Transient Analysis of output

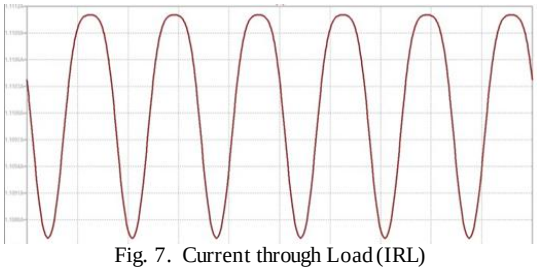

Fig. 7. Current through Load (IRL)

7. Conclusion

Designing a stacked power amplifier has been presented in this project work. The proposed design has been simulated using LT spice tool in 180 nm CMOS process technology with proper specifications, Design, analysis, calculations and simulation results have been provided. Simulated results show the overall signal gain, and power added efficiency of power amplifier has been increased by 34.79%. Power amplifier performances can be improved by selecting an optimal capacitance. In this work linearity and efficiency of the stacked power amplifier is improved.

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